

# EECE574/EECE455 VLSI DESIGN & ARCHITECTURES

SYLLABUS FALL-2009

## **1. Instructor**

Professor Qinru Qiu, Dept. Electrical and Computer Engineering, Room ENGB-P14,  
Tel: (607)777-4918, email: [qqiu@binghamton.edu](mailto:qqiu@binghamton.edu)  
Office Hours: Tuesday 2 – 4pm

## **2. Class Location and Times**

ENGB-J15  
Monday and Wednesday 1:10 pm ~ 2:35 pm

## **3. Books**

- (*Required*) Textbook: J. M. Rabaey, A. Chandrakasan, and B. Nikolic, “Digital Integrated Circuits: a Design Perspective”, 2<sup>nd</sup> edition, Prentice Hall 2003
- (*Optional*) Reference: N. H. E. Weste and K. Eshraghian, “Principles of CMOS VLSI Design: A Systems Perspective”, 2<sup>nd</sup> edition, Addison-Wesley, 1993

## **4. Objectives**

- Ability to understand the functions and the properties of CMOS devices, combinational gates, and sequential circuits
- Ability to analyze the performance and power consumption of a digital VLSI circuit using proper device and interconnect models
- Ability to design functional units such as adders and multipliers using CMOS devices
- Ability to optimize a digital circuit with respect to different quality metrics such as cost, speed, power dissipation, and reliability
- Ability to use Cadence layout design tool and HSPICE for VLSI circuit design and analysis

## **5. Topics**

- Introductions
- CMOS devices
- The manufacturing process
- Cadence and HSPICE tutorial
- Wire modeling
- CMOS inverter
- Combinational logic gates
- Designing arithmetic blocks
- Sequential logic gates
- Implementation strategies
- Digital circuit timing analysis
- Designing memory blocks

## **6. Background Requirements**

This class will need a background in digital circuit design and linear circuit analysis.

## **7. Project**

16 bits carry bypass adder

## **8. Student Evaluation**

- Homework: 20%

- Project: 35%
- Midterm: 25%
- Final: 20%

**9. Academic Honor Code**

All students should read and abide the student academic integrity policy, which is published in BU's "*Student Handbook*".